WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a cell transistor including:

a pair of source and drain regions formed in a surface portion of a silicon substrate so as to have a predetermined space therebetween;

a channel region sandwiched by the source and drain regions;

a gate formed above the channel region with a gate dielectric film being formed therebetween; and

a silicon plug formed on the silicon substrate, the silicon plug electrically contacting the source and drain regions, an upper portion of the silicon plug being a first self-aligned silicide portion.

2. The semiconductor device according to claim 1, comprising a memory cell portion including a plurality of first transistors and a periphery circuit portion including at least one second transistor for activating the memory cells, wherein each of the first transistors corresponds to the cell transistor.

3. The semiconductor device according to claim 2, wherein surface portions of the silicon substrate serving as surface portions of the source and drain regions of the second transistor in the periphery circuit portion serve as second self-aligned silicide portions, and a height of the second self-aligned silicide portions is different from a height of the first self-aligned silicide portion.

4. The semiconductor device according to claim 1, wherein a wiring line is connected to a predetermined

first self-aligned silicide portion.

5. The semiconductor device according to claim 2, wherein an upper portion of a gate of at least one of the first transistor and the second transistor is changed to a self-aligned silicide.

6. The semiconductor device according to claim 5, wherein the upper portion of the gate of the first transistor is not changed to a self-aligned silicide, and the upper portion of the gate of the second transistor is changed to a self-aligned silicide.

7. The semiconductor device according to claim 2, wherein neither an upper portion of the first transistor nor an upper portion of the second transistor is changed to a self-aligned silicide.

8. The semiconductor device according to claim 1, wherein the silicon substrate is an SOI substrate.

9. The semiconductor device according to claim 8, comprising a memory cell portion including a plurality of first transistors and a periphery circuit portion including at least one second transistor for activating the memory cells, wherein each of the first transistors corresponds to the cell transistor.

10. The semiconductor device according to claim 9, wherein surface portions of the silicon substrate serving as surface portions of the source and drain regions of the second transistor in the periphery circuit portion serve as second self-aligned silicide portions, and a height of the second self-aligned silicide portions is different from a height of the first self-aligned silicide portion.

11. The semiconductor device according to claim 8, wherein a wiring line is connected to a predetermined first self-aligned silicide portion.

12. The semiconductor device according to claim 8, wherein an upper portion of a gate of at least one of the first transistor and the second transistor is changed to a self-aligned silicide.

13. The semiconductor device according to claim 12, wherein the upper portion of the gate of the first transistor is not changed to a self-aligned silicide, and the upper portion of the gate of the second transistor is changed to a self-aligned silicide.

14. The semiconductor device according to claim 1, wherein the silicon substrate is a bulk silicon substrate.

15. The semiconductor device according to claim 14, comprising a memory cell portion including a plurality of first transistors and a periphery circuit portion including at least one second transistor for activating the memory cells, wherein each of the first transistors corresponds to the cell transistor.

16. The semiconductor device according to claim 15, wherein surface portions of the silicon substrate serving as surface portions of the source and drain regions of the second transistor in the periphery circuit portion serve as second self-aligned silicide portions, and a height of the second self-aligned silicide portions is different from a height of the first self-aligned silicide portion.

17. The semiconductor device according to claim 14, wherein a wiring line is connected to a predetermined first self-aligned silicide portion.

18. The semiconductor device according to claim 14, wherein an upper portion of a gate of at least one of the first transistor and the second transistor is changed to a self-aligned silicide.

19. The semiconductor device according to claim 18, wherein the upper portion of the gate of the first transistor is not changed to a self-aligned silicide, and the upper portion of the gate of the second transistor is changed to a self-aligned silicide.

20. A method of manufacturing a semiconductor device comprising:

forming a pair of source and drain region on a silicon substrate with a predetermined space being held therebetween;

forming a gate on a channel region sandwiched by the source and drain regions with a gate dielectric film provided between the channel region and the gate; and

changing an upper portion of a silicon plug thus formed to a self-aligned silicide.